

2

HDL-TM-91-9

July 1991

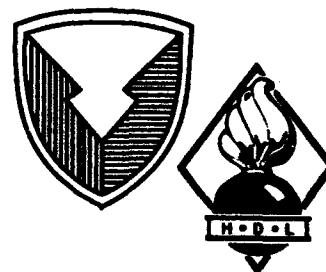
**AD-A241 974**



**Development of a Shadow Mask for Sputtering Platinum  
onto Ferroelectric-Coated Substrates**

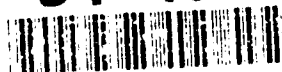
by Judith T. McCullen  
Bernard J. Rod  
Robert Reams

**DTIC**  
**ELECTE**  
**OCT 22 1991**  
**S B D**



**U.S. Army Laboratory Command**  
**Harry Diamond Laboratories**  
Adelphi, MD 20783-1197

**91-13634**



Approved for public release; distribution unlimited.

21 061

The findings in this report are not to be construed as an official Department of the Army position unless so designated by other authorized documents.

Citation of manufacturer's or trade names does not constitute an official endorsement or approval of the use thereof.

Destroy this report when it is no longer needed. Do not return it to the originator.

REPORT DOCUMENTATION PAGE			Form Approved OMB No. 0704-0188	
<small>Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing the burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503.</small>				
1. AGENCY USE ONLY (Leave blank)		2. REPORT DATE July 1991		3. REPORT TYPE AND DATES COVERED Progress, from Jan to May 1990
4. TITLE AND SUBTITLE Development of a Shadow Mask for Sputtering Platinum onto Ferroelectric-Coated Substrates			5. FUNDING NUMBERS PE: 62120	
6. AUTHOR(S) Judith T. McCullen, Bernard J. Rod, and Robert Reams				
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Harry Diamond Laboratories 2800 Powder Mill Road Adelphi, MD 20783-1197			8. PERFORMING ORGANIZATION REPORT NUMBER HDL-TM-91-9	
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) U.S. Army Laboratory Command 2800 Powder Mill Road Adelphi, MD 20783-1145			10. SPONSORING/MONITORING AGENCY REPORT NUMBER	
11. SUPPLEMENTARY NOTES AMS code: 612120 H250011 HDL PR: 1XE723				
12a. DISTRIBUTION AVAILABILITY STATEMENT Approved for public release; distribution unlimited			12b. DISTRIBUTION CODE	
13. ABSTRACT (Maximum 200 words)  The Army has a continuing requirement for nonvolatile memories in which critical information placed in system memory is available after the system is reactivated following storage or power down. To meet the needs of future increases in memory size and a requirement for nonvolatile random access memory devices, ferroelectric thin film material research and development has become a priority. Ferroelectric nonvolatile memories combine the advantages of CMOS circuitry, small size, and low power with the ability to retain information in a power-off condition over long periods of time (years). In support of the ferroelectric memory program, a project was undertaken to make a shadow mask for sputter-depositing platinum electrodes with microfabrication techniques to create very small shaped openings through a silicon wafer. The mask is designed so that electrode material such as platinum sputtered through the mask onto a ferroelectric thin film substrate creates small well-defined capacitors that can then be used for extensive ferroelectric material research.				
14. SUBJECT TERMS Photolithography, shadow mask, ferroelectric, sputtering			15. NUMBER OF PAGES 20	
			16. PRICE CODE	
17. SECURITY CLASSIFICATION OF REPORT Unclassified	18. SECURITY CLASSIFICATION OF THIS PAGE Unclassified	19. SECURITY CLASSIFICATION OF ABSTRACT Unclassified	20. LIMITATION OF ABSTRACT UL	

# Contents

	Page
1. Introduction .....	5
2. Factors Considered in Fabricating Shadow Mask .....	6
3. Testing and Evaluation .....	8
4. Results and Conclusions .....	9
Acknowledgements .....	13
References .....	14
Distribution .....	15

# Figures

1. Cross-section of PZT capacitor .....	6
2. Side view of etch angle .....	7
3. Top view of etch angle .....	7
4. Profile for etch calculation .....	8
5. Holes etched in 51- $\mu$ m-thick wafer using patterned squares .....	10
6. Holes etched through 51- $\mu$ m-thick wafer using patterned circles .....	11
7. Undercutting of circular pattern along crystal planes .....	11
8. Squares etched through 279- $\mu$ m-thick wafer using patterned circles .....	12
9. Platinum squares sputtered through etch-through shadow mask .....	12
10. Platinum dots sputtered through metal screen .....	13

Accession For	
NTIS GRA&I	<input checked="" type="checkbox"/>
DTIC TAB	<input type="checkbox"/>
Unannounced	<input type="checkbox"/>
Justification	
By	
Distribution/	
Availability Codes	
Dist	Avail and/or Special
A-1	



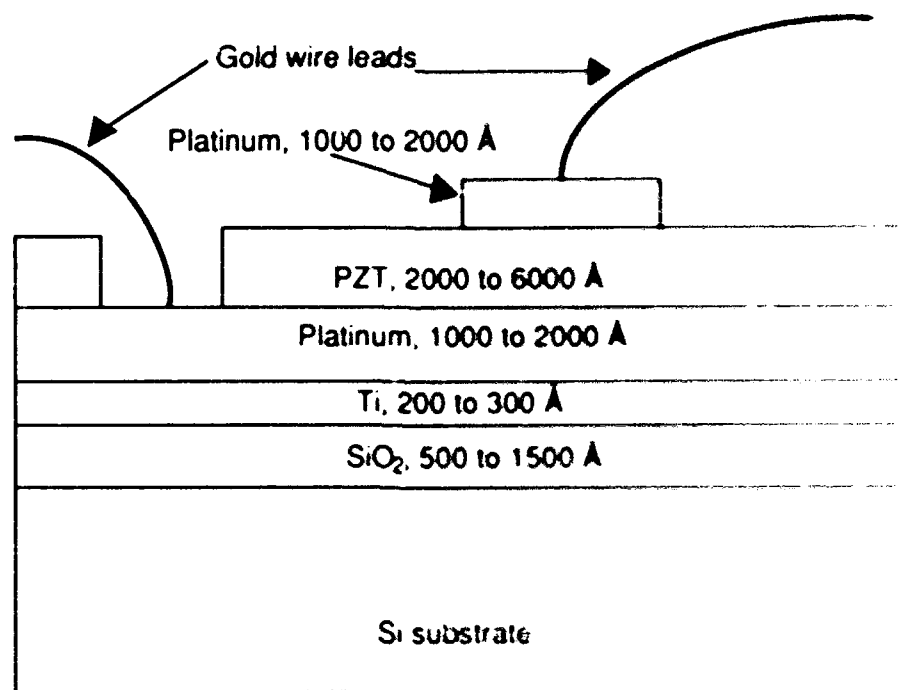
# 1. Introduction

Ferroelectric thin films are being investigated as a nonvolatile storage material for fabricating high-density random access memory devices that are able to retain information over long periods without applied power. Memory cell size reduction is an essential part of achieving the substantial increase in the number of memory cells that is projected to be needed for the future designs required by sophisticated Army electronic systems. This reduction in size requires a ferroelectric material that possesses a significantly higher dielectric constant and dielectric reliability [1] than is presently available with the standard silicon dioxide dielectric layers, which in turn has resulted in an increased interest in ferroelectric materials research. Although there are over 1400 known (bulk) ferroelectric materials, most of these exhibit characteristics that are not conducive to use in fabricating integrated circuits [2].

Research into ferroelectric materials is made easier by the evaluation of capacitors fabricated with sol gel spin on PZT (lead zirconate titanate) thin film ferroelectric material. Ferroelectric materials by definition are polar structural phase materials that change phase at a characteristic transition temperature, accounting for spontaneous polarization reversal capabilities and therefore large storage-charge densities [1]. Detailed time-dependent measurements help clarify the causes of degradation of PZT properties due to fatigue and aging to determine the efficacy of using sol gel spin on PZT material for producing a ferroelectric device chip. The ferroelectric device chip will then be fabricated for radiation and reliability testing, and the results will be used to further aid in developing nonvolatile random access memory devices for Army systems.

Ferroelectric capacitors are fabricated with platinum as the top electrode, PZT as the dielectric, and platinum under the PZT to form the bottom plate (fig. 1). To thoroughly evaluate the various PZT materials available, the top platinum has been defined through two different techniques. The first technique involves chemically etching platinum dots after the whole substrate is covered with a platinum film using a selected deposition process (sputtering). The second method requires making a shadow mask whereby the solid mask with patterned windows rests on the substrate and the platinum is then sputtered onto the PZT material through the patterned windows. The second approach is a simple method to create test samples on a quick turnaround (QTA) basis. For our research, the mask was fabricated from a silicon wafer. The process used to develop this shadow mask is the topic of discussion in this report.

Figure 1. Cross-section of PZT capacitor.



## 2. Factors Considered in Fabricating Shadow Mask

The goal of this work was to etch patterned holes through a silicon wafer to create a shadow mask through which platinum would be sputtered onto a PZT-coated substrate. In silicon wafers  $\langle 100 \rangle$  crystal orientation will etch at a much higher rate than  $\langle 111 \rangle$ , a differential of almost 100 to 1 with the potassium hydroxide etch mixture considered here [3]. Thus we see that silicon etches along the crystal plane, depending upon the etch used and the crystal orientation of a particular wafer, and not necessarily perpendicularly through the depth of the wafer (fig. 2 and 3 and fig. 4 (sect. 3)). Therefore the etch and the crystal orientation angle must be used to calculate the surface pattern hole size needed to achieve the desired 127- $\mu\text{m}$ -diam holes in the wafer required by this experiment. The approach here was to etch through  $\langle 100 \rangle$  crystal orientation wafers, both 51- $\mu\text{m}$  thick, with a diameter of 3.175 cm. Also used were wafers with a thickness of 279  $\mu\text{m}$  and a diameter of 5.08 cm (since these were on hand) to determine which would make a better mask.

Three silicon etches were considered for etching through the silicon: a fast-etch mixture of nitric acid, acetic acid, and hydrofluoric acid; a potassium hydroxide etch mixture of potassium hydroxide, normal propanol, and water; and an EDP (ethylenediamine-pyrocatechol) etch mixture. Another consideration, which depended on the etch used, was what material would be suitable to mask the silicon while etching the shadow mask. Photoresist, silicon dioxide, and silicon nitride were all possibilities that were evaluated.



Figure 2. Side view of etch angle: potassium hydroxide etch;  $\langle 100 \rangle$  crystal orientation.

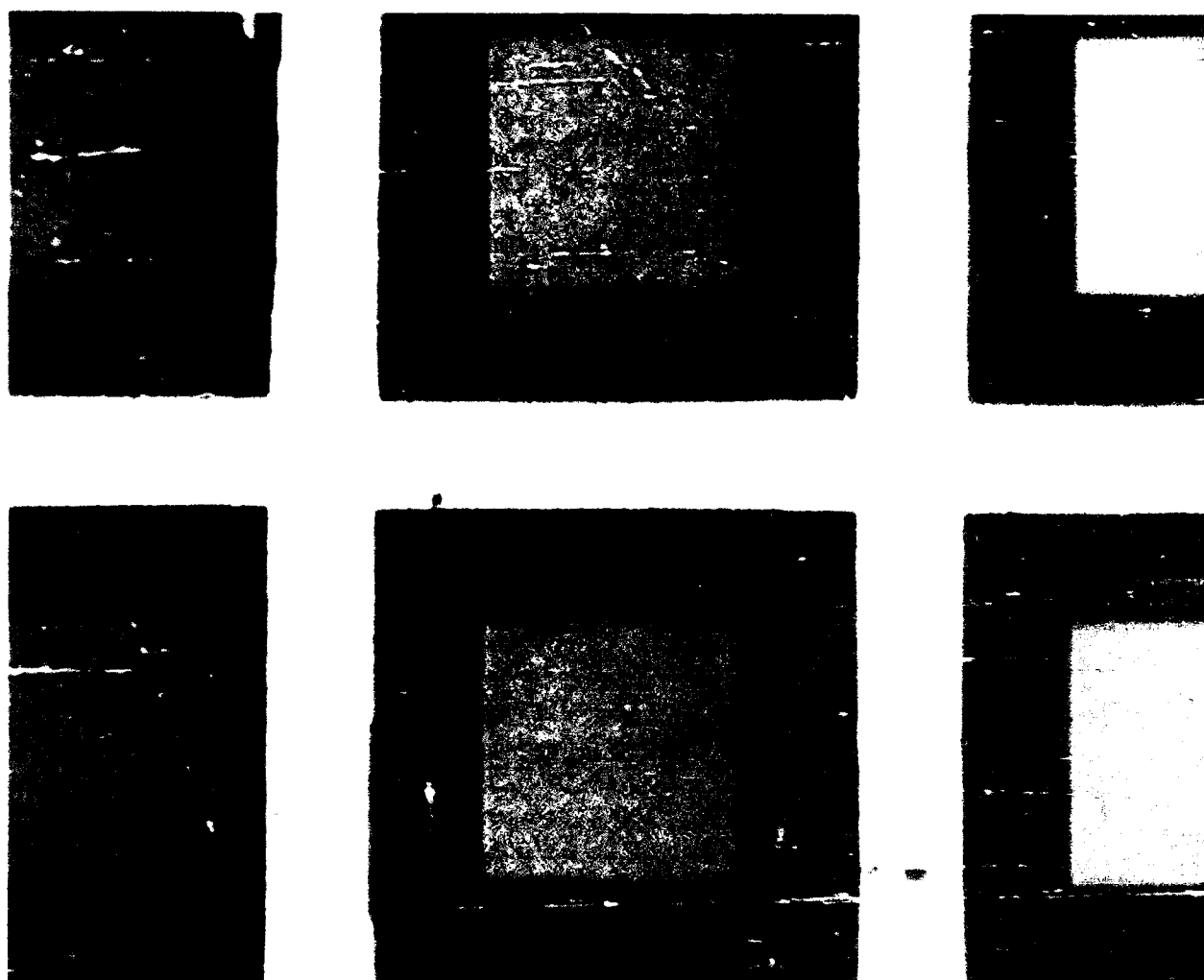


Figure 3. Top view of etch angle: potassium hydroxide etch;  $\langle 100 \rangle$  crystal orientation.

### 3. Testing and Evaluation

The first etch test sample, 279  $\mu\text{m}$  thick, was coated with photoresist both on the polished surface and on the back to mask the silicon from the etch. The polished side was patterned with 533- $\times$ 533- $\mu\text{m}$  squares. The etch used was an isotropic fast etch of 3 parts nitric acid, 2 parts acetic acid, and 1 part hydrofluoric acid, estimated to etch silicon at 12 to 13  $\mu\text{m}$  (120,000 to 130,000  $\text{\AA}$ ) per minute. The photoresist did not hold up in the etch; it lifted in less than one minute and the area of silicon to be protected was etched along with the holes.

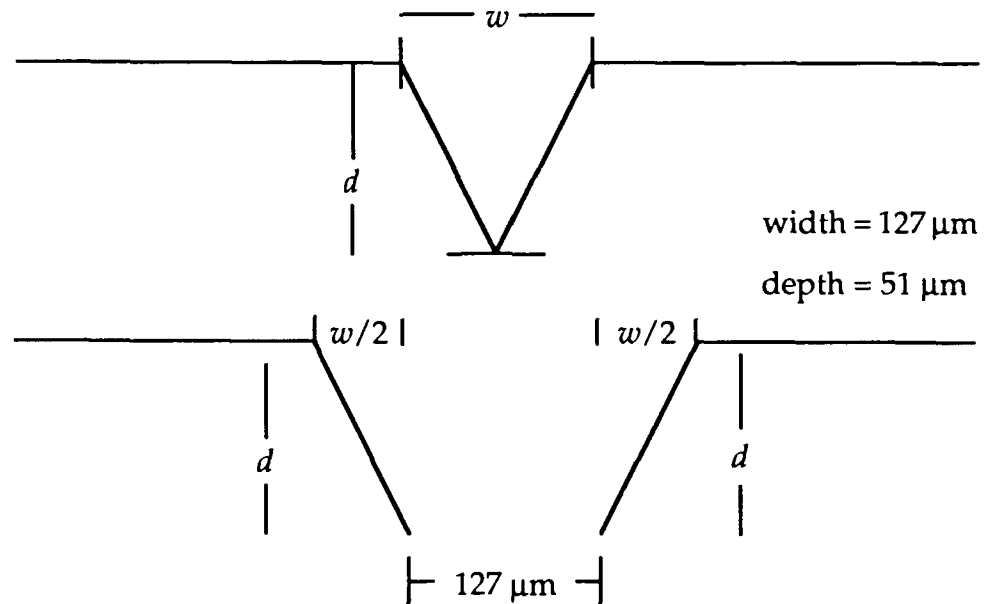
A decision was then made to use an anisotropic potassium hydroxide etch mixture of 80-g normal propanol, 100-g potassium hydroxide, and 320-g deionized water. For several reasons, this is more desirable than the previous fast-acid-based etch, which is isotropic and harder to control when etching thick materials (i.e.,  $\mu\text{m}$  vs  $\text{\AA}$ ). Acid etches tend to etch less uniformly and are more hazardous to work with than caustic etches such as the potassium hydroxide mixture [4].

The surface pattern hole size was calculated for  $\langle 100 \rangle$  crystal orientation wafers using the potassium hydroxide etch mixture, with the following formula, where  $d$  is the etch-through depth and  $w$  is the width of the surface pattern [5]:

$$d = w/2 \tan (54.7^\circ) ;$$

$$\text{therefore, } d = 0.706 w .$$

Figure 4. Profile for etch calculation.





If the thickness (i.e., depth) of the wafer to be etched through is known, the width of the surface pattern can be calculated. The desired hole size must be added to this calculated figure to determine the actual surface pattern width. Using rounded figures,  $533 \pm 533\text{-}\mu\text{m}$  squares were needed to be patterned for  $279\text{-}\mu\text{m}$ -thick etch-through depths and  $203 \times 203\text{-}\mu\text{m}$  squares for  $51\text{-}\mu\text{m}$  depths.

Having used this potassium hydroxide etch mixture in previous work we knew that photoresist does not maintain integrity over time. Thus it was decided to mask the etch with pyrogenically grown silicon dioxide on the samples that measured  $51\text{-}\mu\text{m}$  thick. The polished and back surfaces were coated with photoresist.  $203 \times 203\text{-}\mu\text{m}$  squares were patterned, the silicon dioxide was etched in the patterned area leaving a mask everywhere else including the water back. The resist was removed, and the silicon was etched through in the squares where the silicon dioxide was etched away. Then the silicon dioxide mask was removed. After trying to control the etch rate on several etch-through tests on both  $279\text{-}\mu\text{m}$ -thick and  $51\text{-}\mu\text{m}$ -thick wafers, we could obtain a fast and yet uniform etch rate of  $20,000\text{ }\text{\AA}/\text{min}$  ( $2\text{-}\mu\text{m}/\text{min}$ ) with a potassium hydroxide etch mixture temperature of  $95^\circ\text{C} \pm 5$ .

The silicon dioxide mask was attacked and eventually etched away before penetrating through the  $279\text{-}\mu\text{m}$ -thick silicon samples. We next tested silicon nitride as an etch mask for these thicker samples by first growing a bonding layer of  $800\text{-}\text{\AA}$  silicon dioxide and then depositing  $1000\text{-}\text{\AA}$  silicon nitride. The polished surfaces of each wafer were patterned with  $533 \pm 533\text{-}\mu\text{m}$  squares, the silicon nitride was etched in the patterned areas, the resist was removed, the silicon dioxide was then etched in the patterned area, and then the silicon was etched through the patterned opening. Finally the silicon nitride mask was removed.

## 4. Results and Conclusions

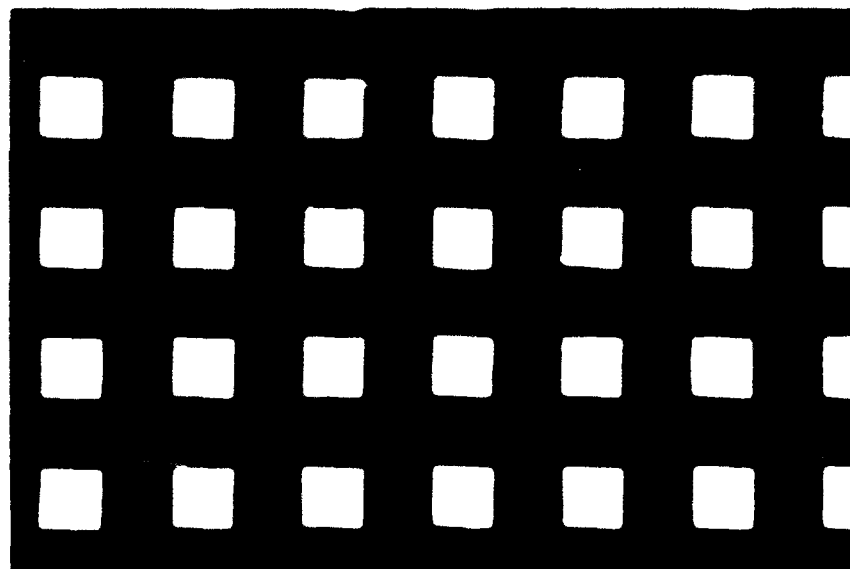
Because of the selectivity of the etch along the crystal planes and the limitations of aligning the pattern exactly parallel to the crystal plane of the wafer, the patterned squares etched unevenly along the edges, i.e., each area that overlapped a plane was attacked by the etch, producing misshapen etched squares (fig. 5).

Holes of  $203\text{-}\mu\text{m}$  diameter were patterned to eliminate having more than one point contact the crystal plane and the resulting etch-through pattern—in spite of slightly shifted rows (due to previously mentioned problem of aligning pattern exactly parallel to crystal plane)—producing more uniformly sized and straight edged squares that measured  $127 \times 127\text{-}\mu\text{m}$  (fig. 6). Undercutting the circular pattern at four arcs of the circle (fig. 7) resulted in the final square pattern, satisfying the

greater potassium hydroxide etch rate at the  $\langle 100 \rangle$  crystallographic plane compared to that of the  $\langle 111 \rangle$  plane. Therefore, round hole patterns were used for all acceptable etch through shadow masks. The squares etched in the 51  $\mu\text{m}$ -thick wafer proved to be acceptably uniform in shape and size and were also closer together, providing many more capacitors on a small sample (fig. 6). Those squares etched in the 279  $\mu\text{m}$ -thick wafers were not uniformly sized and shaped (fig. 8), possibly because the silicon nitride mask started to deteriorate at the end of the long period of time necessary to etch through the thicker silicon. The squares were also farther apart because of the distance apart they needed to be patterned to accommodate the etch angle, resulting in much wasted area on the small test samples (fig. 8). Platinum was sputtered through the 51  $\mu\text{m}$ -thick masks, and the resulting platinum squares were quite well defined (fig. 9). Before using the shadow mask, we attempted to sputter platinum through a metal screen (on hand, but not designed as a metal mask). In this case, the platinum under-shadowed the screen mask, which was too rigid (fig. 10), and the resulting dots were therefore unacceptable.

In conclusion, we have shown that with an appropriate processing sequence based on potassium hydroxide, very acceptable shadow masks can be fabricated from silicon wafers. Thin silicon wafers of about 51 to perhaps 127  $\mu\text{m}$  are more desirable than thicker ones in producing uniform structures. Previous micromachining work done with EDP produced results that were less acceptable than those obtained with the potassium hydroxide and, because EDP is a much more hazardous chemical to use, further EDP process experimentation will not be considered.

Figure 5. Holes etched in 51- $\mu\text{m}$ -thick wafer using patterned squares.



1. The first part of the document is a letter from the President of the United States to the Congress, dated January 1, 1861.

2. The second part is a report from the Secretary of the Treasury, dated January 1, 1861.

Figure 8. Squares etched through 279- $\mu\text{m}$ -thick wafer using patterned circles.

Figure 9. Platinum squares sputtered through etch-through shadow mask.

Figure 10. Platinum dots sputtered through metal screen.

## Acknowledgements

The authors wish to acknowledge Timothy Mermagen for computer graphics herein and Bohdan Dobriansky for his technical assistance in editing this paper.

## References

1. Laureen H. Parker and Allen F. Tasch, *IEEE Circuits and Devices Magazine* (January 1990)
2. J. E. Scott, *Journal of Applied Physics*, **66**, No. 3 (1 August 1989)
3. Stanley Wolf and Richard N. Tubert, *Silicon Processing for the VLSI Era, Vol. 1: Process Technology*, Lattice Press (1986)
4. *J. Electrochemical Society*, **136**, No. 10, The Electrochemical Society, Inc. (October 1989)
5. Roy A. Coldeset, *Microelectronics Processing and Device Design*, New York: John Wiley and Sons, Inc. (1983)

## DISTRIBUTION

Administrator  
Defense Technical Information Center  
Attn DTIC-DDA (2 copies)  
Cameron Station, Building 5  
Alexandria, VA 22304-6145

Director  
Defense Advanced Research Projects Agency  
Attn Dir, Material Sciences  
Attn Dir, Strategic Technology Office  
Attn Dir, Technology Assessments Office  
Attn Tech Info Office  
1400 Wilson Blvd  
Arlington, VA 22290

Director  
Defense Communications Agency  
Attn Technical Director (B102)  
National Military Command System Support  
Washington, DC 20305

Director  
Defense Communications Engineering Center  
Attn Code R123, Technical Library  
1860 Wiehle Ave  
Reston, VA 22090

Director  
Defense Intelligence Agency  
Attn DS-4A2  
Washington, DC 20301

Director  
Defense Nuclear Agency  
Attn RAEE, LTC A. Constantine  
Attn RAEE, MAJ G. Kweder  
Attn RAEE, L. Palkuti  
Attn RAEE, LCDR L. Cohn  
Attn TITL, Technical Library Div  
6801 Telegraph RD  
Alexandria, VA 22310-3398

Commander  
Field Command, Defense Nuclear Agency  
Attn FCPR  
Kirtland AFB, OH 87115

Director  
National Security Agency  
Attn TDL  
Ft George G. Meade, MD 20755

Under Secretary of Defense for Research  
& Engineering  
Attn Research & Advanced Tech  
Attn Asst to Sec/Atomic Energy  
Attn Dep Asst Sec/Energy Environment & Safety  
Attn Dep Under Sec/Res & Advanced Tech  
Attn Dep Under Sec/Test & Evaluation  
Department of Defense  
Washington, DC 20301

Director  
US Army Electronics Technology & Devices  
Lab, LABCOM  
Attn SLCET-E, Electronic Mat Res Div  
Ft Monmouth, NJ 07703-5601

Commander, US Army  
Armament Munitions & Chemical  
(AMCCOM) R&D Command  
Attn SMCAR-TSS, STINFO Div  
Dover, NJ 07801

Commander  
Atmospheric Sciences Laboratory  
Attn Technical Library  
White Sands Missile Range, NM 88002

## DISTRIBUTION (cont'd)

Ballistic Missile Defense Program  
Management Office  
Attn Technology Dir  
5001 Eisenhower Ave  
Alexandria, VA 22333-0001

Director  
Night Vision & Electro-Optics Laboratory,  
LABCOM  
Attn AMSEL-TMS-IO, Information Ofc  
Attn AMSEL-SI, Electronics Team  
Ft Belvoir, VA 22060

Commander  
Office of Missile Electronic Warfare  
Attn Tech & Adv Concepts Div  
White Sands Missile Range, NM 88002

Director  
Signals Warfare Lab, VHFS  
Attn AMSEL-RD-SW-OPI, Tac Sys Div  
Warrenton, VA 22186-5100

Commander  
CECOM R&D Tech Library  
Attn ASQNC-ELC-IS-L-R  
Ft Monmouth, NJ 07703-5018

Commander  
TRASANA  
Attn ATAA-EAC  
White Sands Missile Range, NM 88002

Commander  
US Armament Munitions & Chemical R&D  
(AMCCOM) Command  
Attn SMCAR-LCN, Nuclear & Fuze Div  
Attn SMCAR-NC, Nuclear/Chemical Surety GP  
Dover, NJ 07801

Commander  
US Army Headquarters Armament, Munitions  
& Chemical Command  
Attn AMSMC-IMF-L/Tech Library  
Rock Island, IL 61299-6000

Director  
US Army Ballistic Research Laboratory  
Attn SLCBR  
Attn SLCBR-AM  
Attn SLCBR-X  
Attn SLCBR-TB-VL  
Aberdeen Proving Ground, MD 21005-5066

Commander  
US Army Communications Command  
Attn Tech Lib  
Ft Huachuca, AZ 85613

Chief  
US Army Communications  
Systems Agency  
Attn SCCM-AD-SV, Library  
Ft Monmouth, NJ 07703

Director  
US Army Electronic Warfare Laboratory,  
LABCOM  
Attn SLCET-D, Electronic Technology  
& Devices Lab  
Attn ASQNC-ELC-IS, Information Services  
Div  
Ft Monmouth, NJ 07703-5601

Director  
US Army Electronics Technology & Devices  
Lab, LABCOM  
Attn SLCET-ER  
Attn SLCET-ER-S  
Attn SLCET-I, Microelectronics  
Attn SLCET-IA  
Ft Monmouth, NJ 07703-5601



## DISTRIBUTION (cont'd)

Commandant  
US Army Engineer Center & School  
Attn Library  
Ft Belvoir, VA 22060-5291

Commander  
US Army Materiel Command  
Attn AMCDE, Dir for Dev & Engr  
Attn AMCDE-R, Sys Eval & Testing  
Attn AMCNC, Nuclear-Chemical Ofc  
5001 Eisenhower Ave  
Alexandria, VA 22333-0001

US Army Materiel Systems Analysis Activity  
Attn AMXSU-MP  
Aberdeen Proving Ground, MD 21005

Commander  
US Army Missile Command  
Attn AMCPM-LCEX  
Attn AMCPM-MDTI  
Attn AMCPM-PE-EA  
Attn AMSMI-RGP  
Attn Army Missile RDE Lab  
Attn Tech Lib  
Redstone Arsenal, AL 35898-5000

Commander  
US Army Missile & Munitions Center &  
School  
Attn ATSK-CTD-F  
Redstone Arsenal, AL 35809

US Army Night Vision & Electro-Optics  
Laboratory  
Attn Technical Library  
Ft Belvoir, VA 22060

Commander  
US Army Nuclear & Chemical Agency  
Attn ATCN-W, Weapons Effects Div

Commander  
US Army Nuclear & Chemical Agency (cont'd)  
Attn Technical Library  
7500 Backlick Road, Building 2073  
Springfield, VA 22150

US Army Strategic Defense Command  
Attn C. Harper, CSSD-SD-YA  
Attn A. Kuehl  
Attn D. Stott  
Attn Library  
PO Box 1500  
Huntsville, AL 35807

Commander  
US Army Tank-Automotive Command  
Attn AMSTA-GCM-SW  
Warren, MI 48397-5000

Commander  
US Army Test & Evaluation Command  
Attn AMSTE-CM-F  
Attn AMSTE-EO  
Attn AMSTE-TO-O, Test Operations Div  
Aberdeen Proving Ground, MD 21005-5055

Commander  
White Sands Missile Range  
Attn STEWS-TE-NT  
White Sands Missile Range, NM 88002

Director  
Naval Research Laboratory  
Attn Code 2620, Tech Library Br  
Washington, DC 20375

US Navy  
Naval Research Laboratory  
Attn 6601  
Attn Code 2627  
Attn Code 4000, Research Dept

## DISTRIBUTION (cont'd)

US Navy  
Naval Research Laboratory (cont'd)  
Attn Code 4004  
Attn Code 5210  
Attn Code 6440  
Attn Code 6620, Radiation Effects  
Attn Code 6627  
Attn Code 6631, J. C. Ritter  
Attn Code 6816  
Attn Code 7701  
4555 Overlook Ave, SW  
Washington DC 20375

Commander  
Naval Surface Weapons Center  
Attn Code WA501, Navy Nuc Prgms Ofc  
Attn Code WA52  
Attn E-43, Technical Library  
Attn WA50  
White Oak, MD 20910

Commander  
Naval Surface Weapons Center  
Attn Code WR, Research & Technology Dept  
Attn DX-21 Library Div  
Attn J. Bean  
Dahlgren Laboratory  
Dahlgren, VA 22448

Director  
AF Avionics Laboratory  
Attn AAT, M. Friar  
Attn DH, LTC McKenzie  
Attn DHE, H. J. Hennecke  
Attn DHM, C. Friend  
Attn TE, Electronic Technology Div  
Attn TER, Electronic Res BR  
Attn TSR, STINFO BR  
Wright-Patterson AFB, OH 45433

Commander  
HQ, USAF/SAMI  
Washington, DC 20330

Director  
Interservice Nuclear Weapons School  
Kirtland AFB, NM 87115

Director  
Joint Strategic Target Planning Staff, JCS  
Attn JLTW-2  
Offutt AFB  
Omaha, NB 68113

Rome Air Development Center  
AF Deputy for Elec Tech  
Attn ESR, W. Shedd  
Hanscom Field  
Bedford, MA 01731

Director  
Armed Forces Radiobiology Research Institute  
Defense Nuclear Agency  
Attn Technical Library  
National Naval Medical Center  
Bethesda, MD 20014

Central Intelligence Agency  
Attn RD/SI, Rm 5G48, HQ Bldg  
Washington, DC 20505

Dept of Energy  
Attn Asst Admin for Nuclear Energy  
Attn Div of Reactor Res & Dev  
Attn Div of Space Nuclear Systems  
Washington, DC 20545

Dept of Energy  
Attn Technical Information Organization  
PO Box 62  
Oak Ridge, TN 37830

## DISTRIBUTION (cont'd)

Dept of Energy  
Albuquerque Operations  
Attn Director  
PO Box 5400  
Albuquerque, NM 87115

Director  
NASA, Goddard Space Flight Center  
Attn 250, Tech Info Div  
Greenbelt, MD 20771

Administrator  
NASA Headquarters  
Attn Ofc of Aeronautics & Space Technology  
Washington, DC 20546

Office of the Deputy Chief of Staff for Research,  
Dev, & Acquisition  
Attn DAMA-ARZ-D, Research Programs  
Attn DAMA-CSS-D, R&D Team  
Attn DAMA-RAX, Sys Review & Analysis Ofc  
Attn Dir of Army Res  
Washington, DC 20310

US Department of Commerce  
Attn Assistant Secretary for Science  
& Technology  
Washington, DC 20230

Director  
Argonne National Laboratory  
9700 South Cass Ave  
Argonne, IL 60439

Director  
Brookhaven National Laboratory  
Associated Universities, Inc  
Upton, Long Island, NY 11973

Jet Propulsion Laboratory  
California Institute of Technology  
Attn D. J. Nichols, T-1180

Jet Propulsion Laboratory (cont'd)  
California Institute of Technology  
Attn Technical Library  
4800 Oak Grove Drive  
Pasadena, CA 91103

Engineering Societies Library  
Attn Acquisitions Dept  
345 E. 47th Street  
New York, NY 10017

Honeywell Incorporated  
Government & Aeronautical Products Div  
Attn J. Schrankler  
2600 Ridgeway Parkway  
Minneapolis, MN 55413

Harris Corporation  
Government Systems Group  
Attn W. E. Abare, MS 20-2604  
PO Box 94000, MS 101/4825  
Melbourne, FL 32902

Kaman Tempo  
Attn C. Fore  
2560 Huntington Ave, Suite 506  
Alexandria, VA 22303

Mission Research Corp  
Attn E. Enlow  
Attn R. Pease  
1720 Randolph Rd, SE  
Albuquerque, NM 87106-4245

Mitre Corp  
Attn M. F. Fitzgerald  
Attn Library  
PO Box 208  
Bedford, MA 01730

## DISTRIBUTION (cont'd)

Sandia National Laboratories  
Attn Library  
PO Box 5800  
Albuquerque, NM 87185

Teledyne Brown Engineering  
Cummings Research Park  
Attn A. Fenelly  
Huntsville, AL 35807

US Army Laboratory Command  
Attn AMSLC-DL, R. Vitali

Installation Support Activity  
Attn SLCIS-CC, Legal Office

USAISC  
Attn AMSLC-IM-VA, Admin Ser Br  
Attn AMSLC-IM-VP, Tech Pub Br  
(2 copies)

Harry Diamond Laboratories  
Attn Laboratory Directors  
Attn SLCHD-TL, Library (3 copies)  
Attn SLCHD-TL, Library (Woodbridge)  
Attn SLCHD-NW, Chief  
Attn SLCHD-NW-CS, Chief  
Attn SLCHD-NW-E, Chief  
Attn SLCHD-NW-EH, Chief  
Attn SLCHD-NW-EP, Chief

Harry Diamond Laboratories (cont'd)  
Attn SLCHD-NW-ES, Chief  
Attn SLCHD-NW-P, Chief  
Attn SLCHD-NW-R, Chief  
Attn SLCHD-NW-RP, Chief  
Attn SLCHD-NW-RS, Chief  
Attn SLCHD-NW-TN, Chief  
Attn SLCHD-NW-TS, Chief  
Attn SLCHD-D, R. Gilbert  
Attn SLCHD-NW, W. Vault  
Attn SLCHD-NW-EP, J. R. Miletta  
Attn SLCHD-NW-P, D. Davis  
Attn SLCHD-NW-RP, J. Benedetto  
Attn SLCHD-NW-RP, K. W. Bennett  
Attn SLCHD-NW-RP, T. V. Blomquist  
Attn SLCHD-NW-RP, H. Boesch  
Attn SLCHD-NW-RP, B. Geil  
Attn SLCHD-NW-RP, T. Griffin  
Attn SLCHD-NW-RP, A. J. Lelis  
Attn SLCHD-NW-RP, J. M. McGarrity  
Attn SLCHD-NW-RP, B. McLean  
Attn SLCHD-NW-RP, T. Mermagen  
Attn SLCHD-NW-RP, T. Oldham  
Attn SLCHD-NW-RP, R. B. Reams (5 copies)  
Attn SLCHD-NW-RP, B. J. Rod (10 copies)  
Attn SLCHD-NW-RS, H. Brandt  
Attn SLCHD-NW-TS, H. Eisen  
Attn SLCHD-TA-ES, R. Goodman  
Attn SLCHD-NW-RP, J. McCullen (20 copies)